

AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED

REVISION TO 37 CFR 1.121)

Please cancel claims 2, 3 and 10 without prejudice.

1. ~~(CURRENTLY AMENDED)~~ A system for designing an integrated circuit (IC) comprising: ~~a circuit comprising (i):~~ . . .
a functional portion; ~~and (ii)~~
a logic portion connected to said functional portion and
5 configured to detect errors, fix errors or verify fixes of errors
in said ~~function~~ functional portion, wherein said logic portion
includes one or more interfaces; ^{pb}

a debugging/bug fix circuit configured to detect errors
in said logic portion through said one or more interfaces; and
10 a diagnostic architecture using said FPGA core in a
system on a chip design.

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2. (CANCEL)

3. (CANCEL)

4. (CURRENTLY AMENDED) The system according to claim 2
1, wherein said system is further configured to (i) provide ease in

bringing up, (ii) verification and (iii) debugging, each by interconnecting said circuit and said debugging/bug fix circuit.

5. (ORIGINAL) The system according to claim 1, wherein said system is further configured to provide one or more programming options of said circuit.

6. (CURRENTLY AMENDED) The system according to claim 2 1, wherein said system is further configured to allow observation of one or more signals by said debugging/bug fix circuit.

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out.
7. (ORIGINAL) The system according to claim 6, wherein said system is further configured to allow observation of said one or more signals when running in a normal mode.

8. (ORIGINAL) The system according to claim 1, wherein said system is further configured to run in a single step mode.

9. (ORIGINAL) The system according to claim 8, wherein said system is further configured to run in said single step mode when controlled by a gate or a core.

10. (CANCEL)

11. (ORIGINAL) The system according to claim 9, wherein said core is programmable.

12. (CURRENTLY AMENDED) The system according to claim 2 1, wherein said debugging/bug fix circuit comprises a debugging workstation.

13. (CURRENTLY AMENDED) The system according to claim 2 1, wherein said debugging/bug fix circuit is further configured to allow one or more debugging features.

14. (ORIGINAL) The system according to claim 13, wherein said one or more debugging features support triggering and tracing based on one or more internal signals.

15. (ORIGINAL) The system according to claim 13, wherein said one or more debugging features support dynamically changing host register values.

16. (ORIGINAL) The system according to claim 13, wherein said one or more debugging features provide complex monitoring functions.

17. (ORIGINAL) The system according to claim 1, wherein said system is further configured to reduce debugging/verification time and/or improve product time to market.

18. (ORIGINAL) The system according to claim 1, wherein said circuit is further configured to operate in a normal mode and a single step mode.

19. (ORIGINAL) The system according to claim 18, wherein said normal mode is configured to allow said circuit to present one or more internal signals of said functional portion and said single step mode is configured to provide a plurality of
5 signals of said functional portion.

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cont. 20. (ORIGINAL) The system according to claim 18, wherein a scan chain is used to diagnose or fix a bug via the logic portion.

21. (CURRENTLY AMENDED) The system according to claim 18
19, wherein the ~~programmable logic~~ portion is further configured to
bridge^{Fig 5} one or more of said plurality of signals between a plurality
of modules.

22. (ORIGINAL) The system according to claim ~~2~~, wherein said debugging/bug fix circuit and said circuit are configured to generate one or more debugging features.

23. (CURRENTLY AMENDED) The system according to claim ~~2~~ 1, wherein said debugging/bug fix circuit is configured to work with Computer Aided Design (CAD) software to provide one or more diagnostic functions.

24. (ORIGINAL) The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of searching for a specific signal pattern, tracing the internal state machine, triggering on a programmed condition and other appropriate diagnostic functions.

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5 cut,
25. (ORIGINAL) The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of on the fly monitoring of a correctness of a bus protocol, and implementing statistics counting to measure the
5 performance and the testing coverage.

26. (CURRENTLY AMENDED) A method for diagnostics comprising the steps of:

(A) interfacing a chip with ~~a~~ an FPGA core;

(B) presenting one or more internal signals of said

5 chip; and

(C) verifying or fixing bugs in said chip with said one or more internal signals; and

(D) programming the FPGA core to dump data from a host register every N clock cycles.

PS Object spec

27. (ORIGINAL) A computer readable medium configured to store instructions for executing the steps of claim 26.

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at.
Please add the following new claims:

28. (NEW) The method according to claim 26, further comprising:

capturing signals every N clock cycles.

29. The method according to claim 28, further comprising the step of:

dynamically changing the values in said host register.

30. The method according to claim 29, further comprising the step of:

searching for a specific signal pattern.

31. The method according to claim 30, further comprising the step of:

monitoring the correctness of a bus protocol.

32. The method according to claim 31, further comprising the step of:

implementing statistics counting to measure (i) the active time on bus request and (ii) the execution coverage of the internal state machines.

33. The method according to claim 26, further comprising the steps of:

triggering and tracing based on internal signals;

triggering on the specific values of address, data, or

command bus;

dynamically changing the host register values; and

monitoring protocol functions.